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An Approach for Designing and Implementing BER Testbed

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Outline

Introduction

System model

Testbed using CSP

Testbed using FPGA

Summary

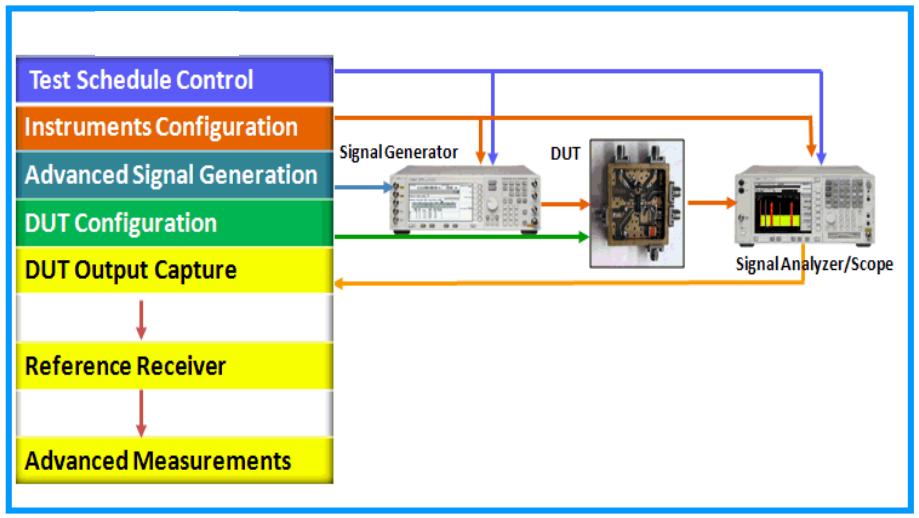
Introduction – How to make a simple Testbed

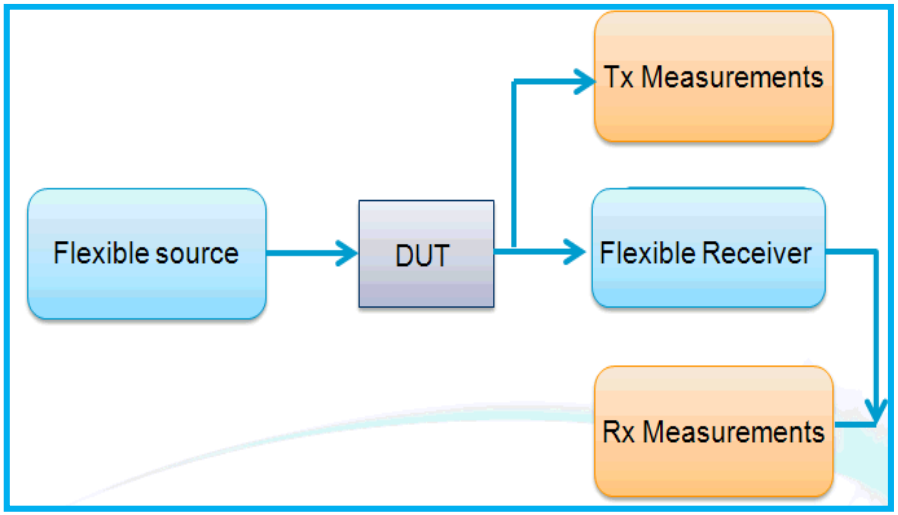
Traditional Way

- Based on HW
- For a specific signal and system
- Hard to switch from one mode to another, that is not good for Milcom systems

New Approach

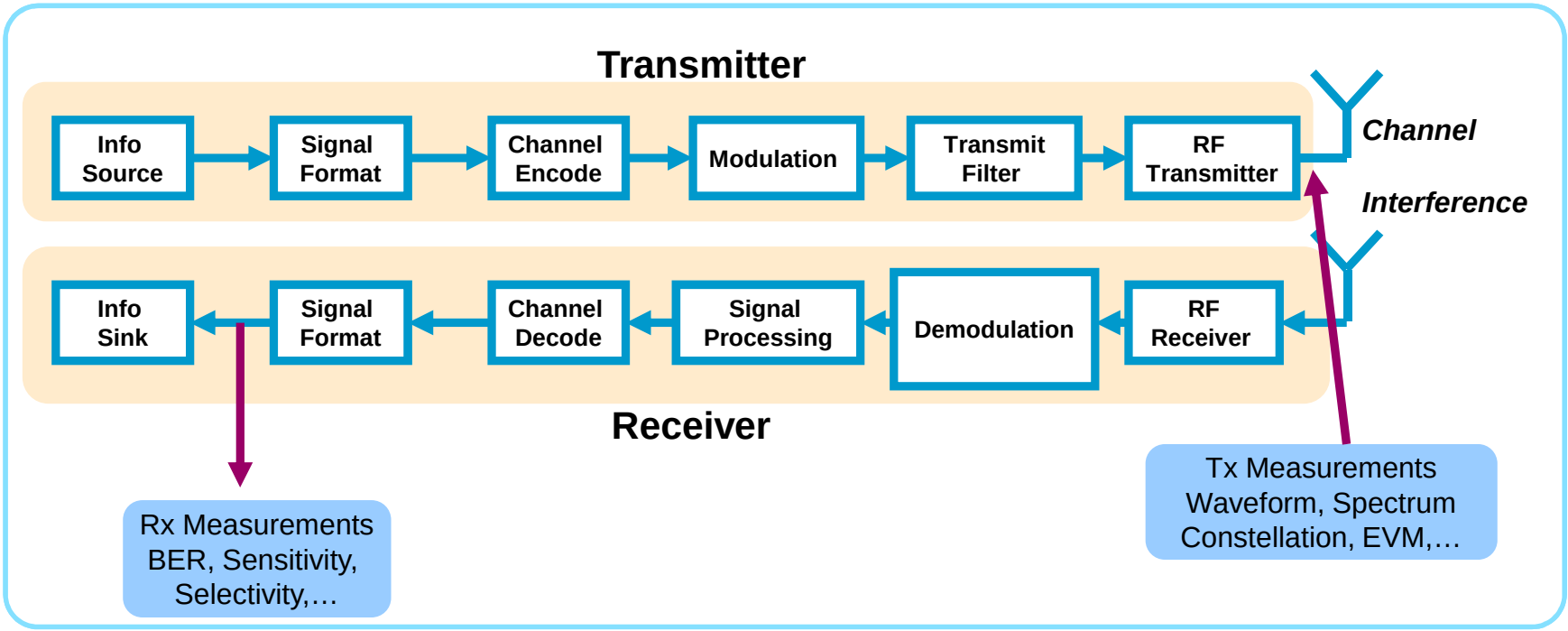
- Reconfigurable for different modes
- Using a Core Software Package (CSP) as a Platform Solution





System Model

- Typical Milcom communication system
- Transmitter, Channel and Receiver are considered
- System performance is measured



Signal Model

The transmission signal can be described as

$$S(t) = A(t)\exp(\ j(2\pi f_c t)) \qquad (1)$$

At the receiver input the equivalent baseband received signal can be described as

$$S(t) = A(t)\exp(j(2\pi f_c t + \alpha + \varphi(t)) + n(t) \qquad (2)$$

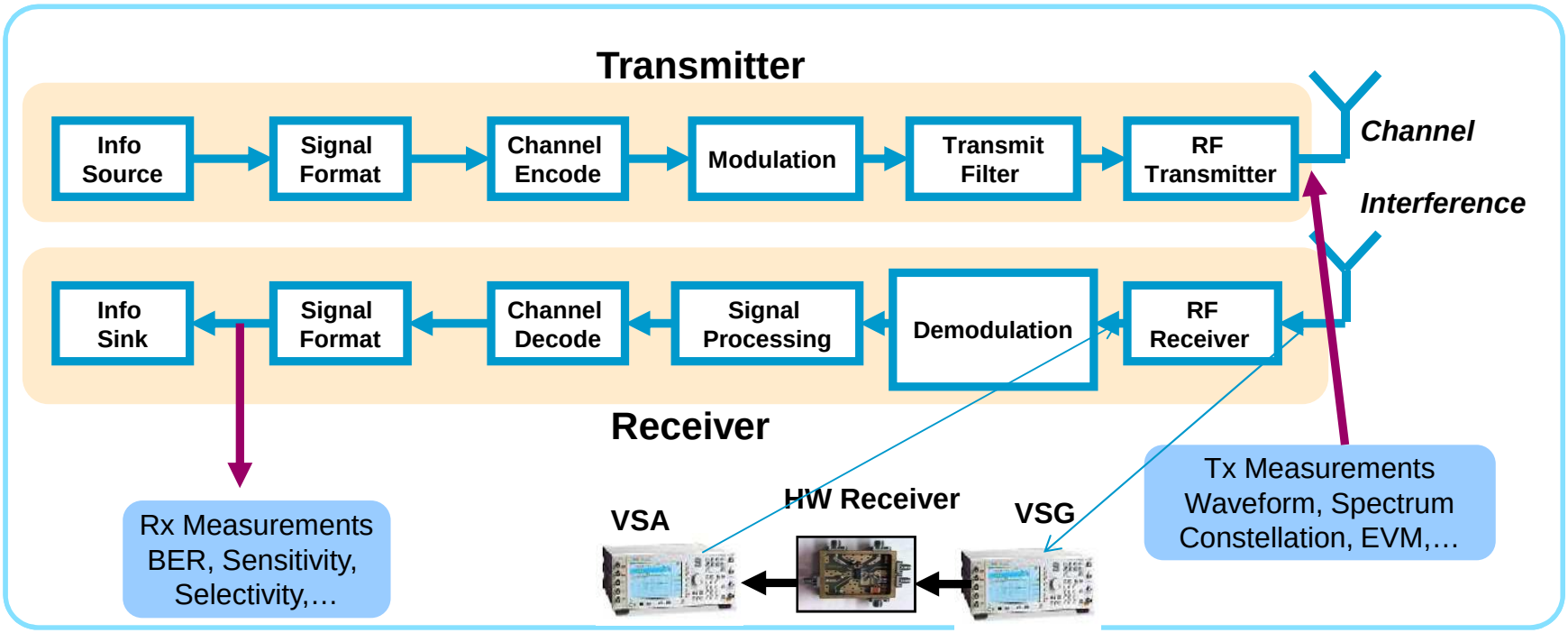
where $A(t)$ is the amplitude of the signal, f_c is the carrier frequency and $\varphi(t)$ is the phase noise caused by the oscillator , $n(t)$ is the channel AWGN noise

Signal Processing algorithm can be implemented in the platform.

As an example, phase error correction algorithm for receiver is introduced in the Signal Processing block with phase error estimator and compensator.

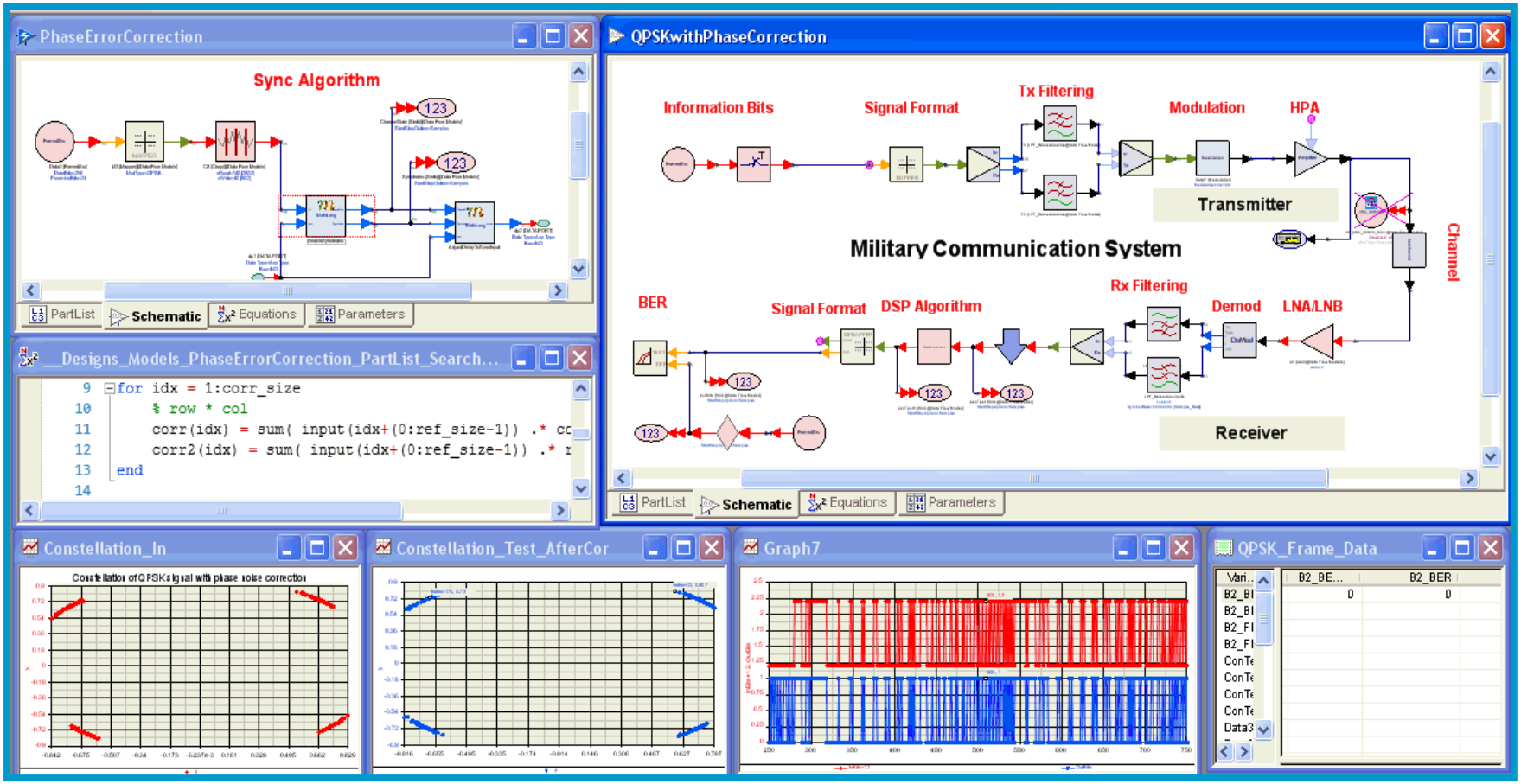
Testbed Based on CSP

1. Create simulation design for test and verification
2. Link to the Instruments to implement the Testbed
3. Hardware Test



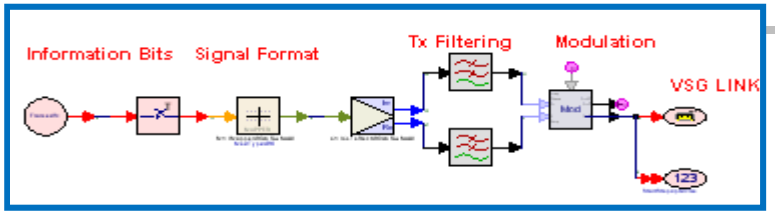
Testbed Based on CSP – QAM example – Step 1

1. Create simulation design for test and verification



Testbed Based on CSP – QAM example – Step 2

2. Link to instruments



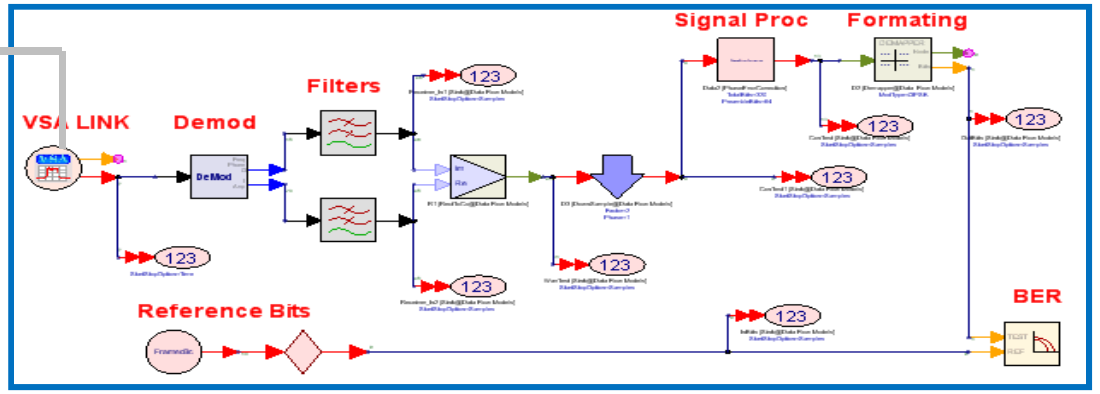
LAN

Antenna

- The QAM signal can be created and verified as a reference transmitter to Test customer's receiver
- The QAM receiver can be created as a reference receiver to Test customer's transmitter
- Through antennas the signal is received by the VSA
- SV capture the received signal process and measure in SV

LAN

Antenna



Testbed Based on CSP – QAM example – Step 3

3. Testing and verification

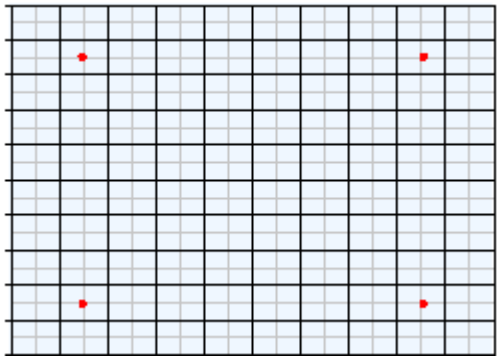


Fig 1. Idea QPSK Constellation

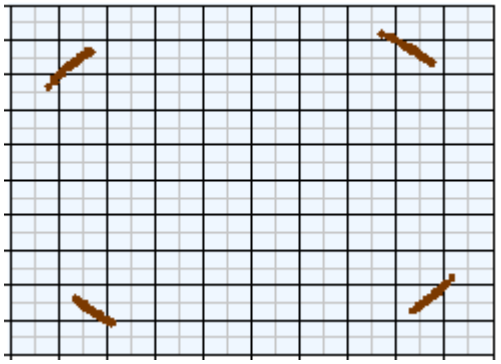


Fig 2. System with phase noise

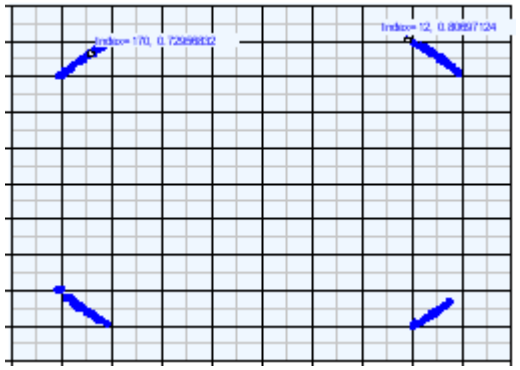


Fig 3. Phase Error is corrected

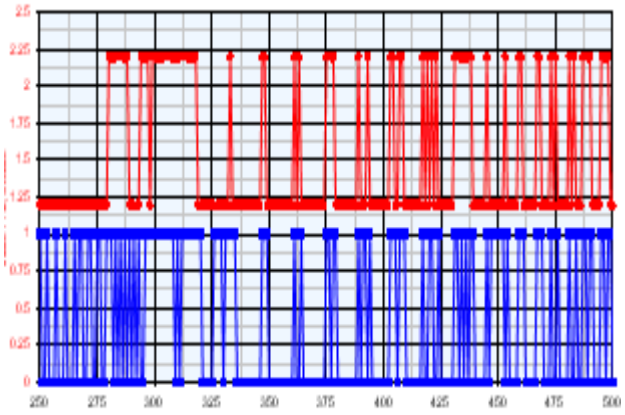


Fig 4. without Phase Error correction

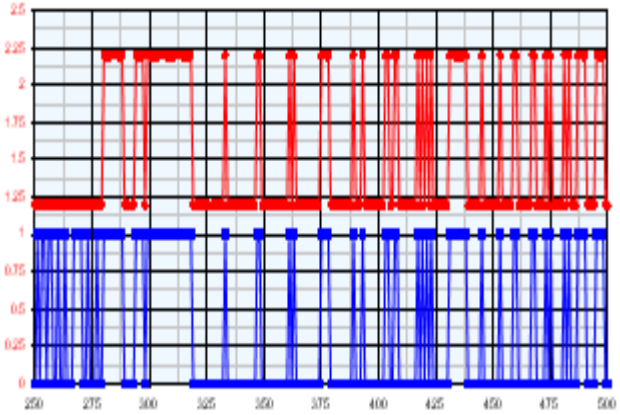


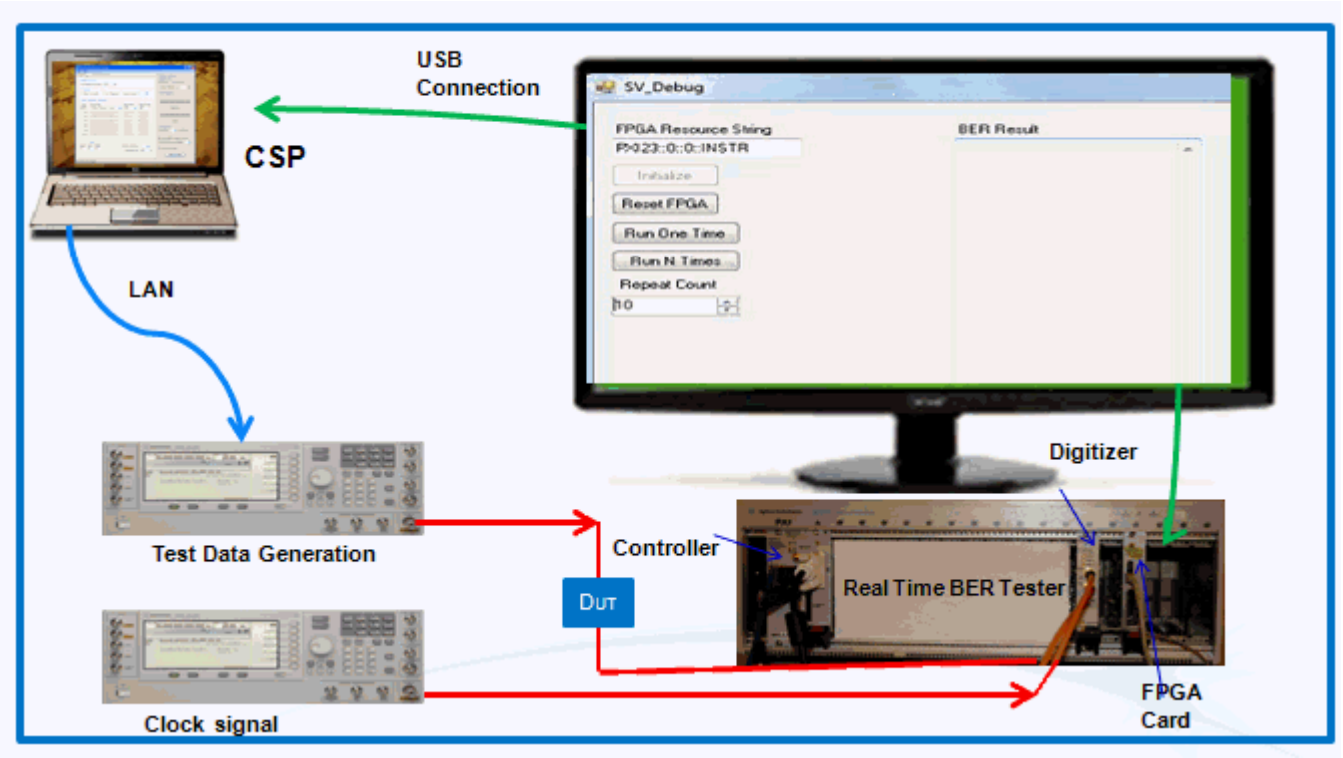
Fig 5. with Phase Error correction

Idea BER for system without noise	With Phase Noise and no PC	With Amplitude plus Phase Noise and no PC	With Phase Noise and PC	With Amplitude plus Phase Noise and PC
0	48%	50.3%	1e-6	2.1 e-5

Fig 6. BER under different conditions

Testbed Based on FPGA

To speed up the BER test, a Testbed using FPGA is designed and implemented for a real time test.



Testbed Based on FPGA

The BER test system includes

- A digitizer to process the input RF/IF test signal
- An FPGA card for the receiver and BER measurement functions
- A control card to pass and display data
- The test signal is generated by instrument. Of course, using CSP in Simulation and then downloading to a VSG is still a possible way.
- Clock signal is generated by another signal generator.

FPGA Receiver – Design and Verification

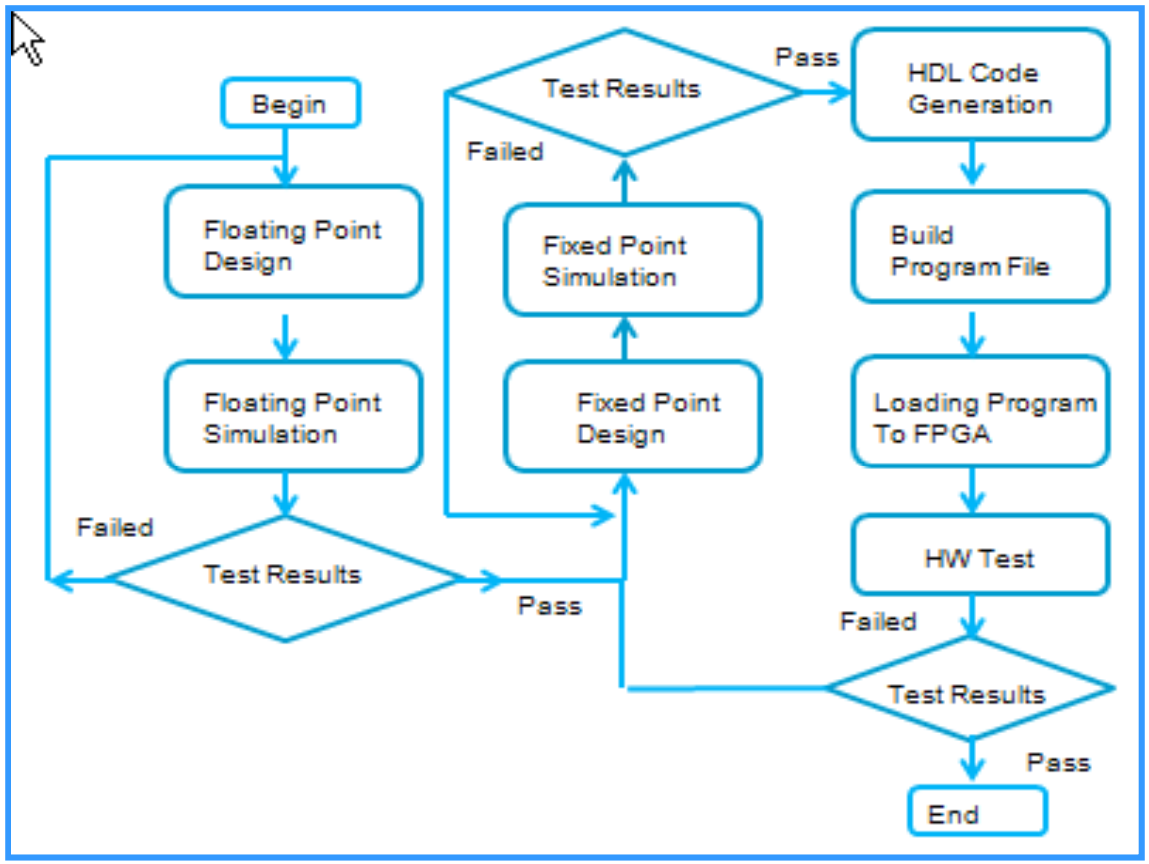


Fig 1. Design Flow for the FPGA Receiver

Testbed Based on FPGA – Example for FSK

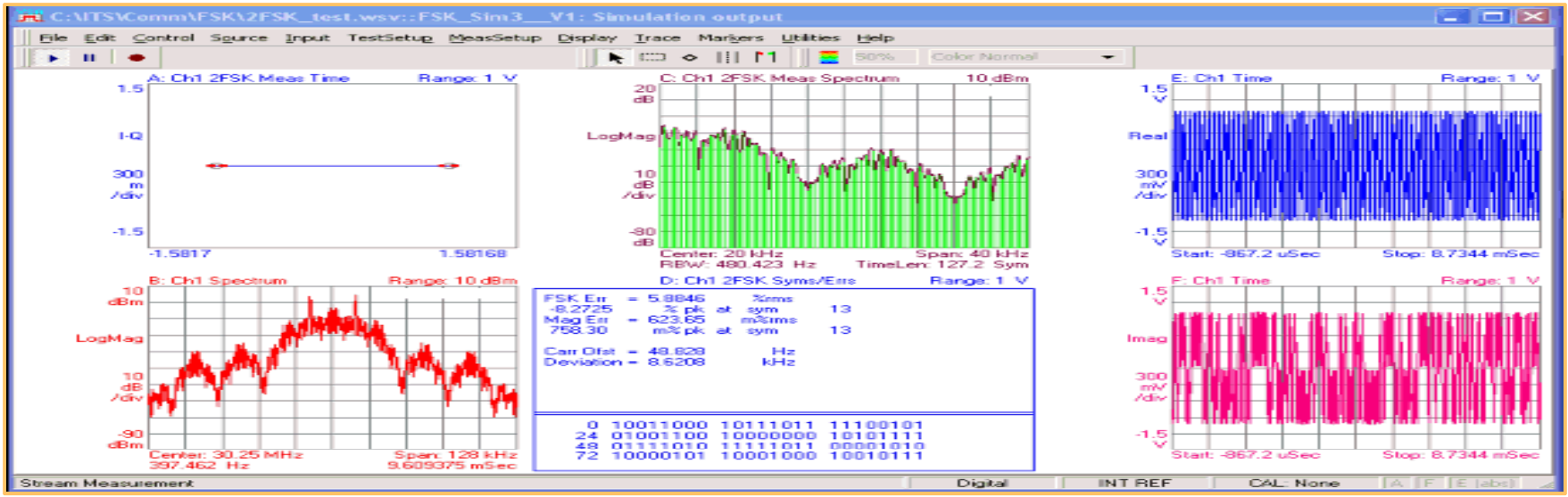


Fig 1. Generate FSK Signal Measured Results for Waveforms, Spectrum, Constellation, …

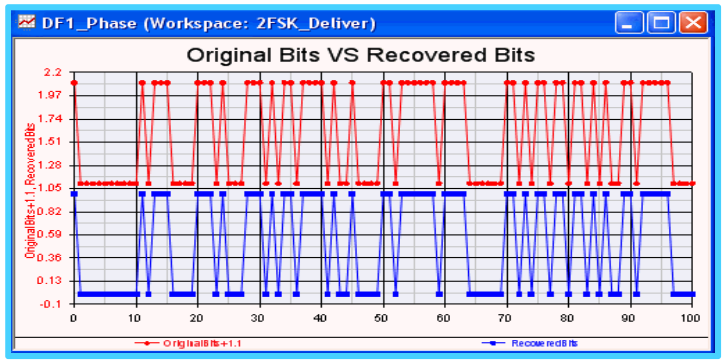


Fig 2. Original bits Vs Recovered Bits

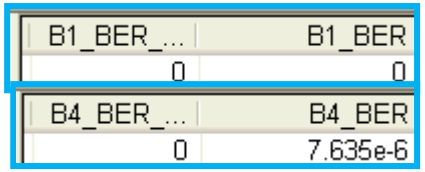


Fig 3. Measured BER

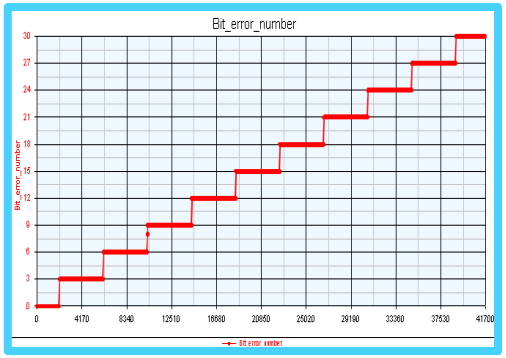


Fig 3. Measured Cumulated Error

Summary and Further Works

- A new approach for designing and implementing BER Testbed has been presented.
- Two ways to build Testbed
  - CSP
    - Gives flexibility to the signal generator, the environment setup and receiver structure.
    - For R&D testing purpose, the CSP can directly construct a Testbed to do the transmission and receiving test as discussed.
  - FPGA
    - A Testbed using FPGA also can be implemented.
    - Real time and easy to use
    - For Manufacture test

Thank You

References

[1] Suzuki, T., Iwai, H., Takeuchi, Y. , Watanabe, F. “A study on receiver performance of a wideband CDMA Testbed system for IMT-2000”, Vehicular Technology Conference, 1999 IEEE 49th, 1732 - 1736 vol.2.
[2] Hannikainen, M.; Vanhatupa, T.; Lemilainen, J.; Saarinen, J., “Windows NT Software Design and Implementation for a Wireless LAN Base Station” ACM International Workshop on Wireless Mobile Multimedia, 1999 (WoWMoM1999), pp. 2-9.
[3] T. H. Lee and A. Hajimiri, "Oscillator Phase Noise: A Tutorial,” IEEE J. Solid-State Circuits, VOL. 35, NO. 3, March 2000.